Methods

Topology

The automatic tuning circuitry (figure 1) is an interface between the coil and the scanner preamplifier. At the press of a button, it measures and adjusts the resonant frequency of the coil to maintain high SNR after changes in the coil and/or load. The circuit has four main blocks: a PLL synthesizer, a phase-comparator, a tune/receive switch, and a microcontroller (MCU) with a digital-to-analog converter (DAC).

Phase-comparator

The phase comparator consists of two ultrafast voltage comparators (part number), a high quality capacitor, a four-quad multiplier (part -), and a RC lowpass filter (figure 3). The capacitor (chosen to have negligible real impedance at the frequency of interest) sits in series with the coil during tuning so that they share the same current. As discussed in ‘Theory if Operation’ (above), the voltage across the capacitor lags the voltage across the coil by [expression] radians. This lag is $\pi/4$ when the coil impedance is purely real (on resonance). By multiplying the voltage across the reference cap with the voltage across the coil, we get a DC component at the output proportional to the cosine of their phase difference. When the lowpass-filtered multiplier output is zero, the coil is resonant. The comparator eliminates the dependance of the multiplier output on its input amplitudes by turning the sinusoidal node voltages into square waves of equal amplitude.

PLL Synthesizer

A PLL synthesizer drives the reference capacitor ($C_{ref}$) and coil with a sinusoidal voltage at the Larmor frequency during tuning mode (figure 2). We use a —— programmable PLL for digital control of the output frequency. We use a 4-pole Butterworth bandpass filter from the PLL datasheet, and a minicircuits VCO. A ——- current feedback amplifier buffers the synthesized signal and drives the load.

Tune/Receive Switch

Signal reception requires isolation of the MR signal from the autotuning circuitry. Likewise, tuning requires isolation of the coil from the preamplifier. The circuit in figure 4 accomplishes both using PIN diodes, and logic control from the MCU. With only passive devices in the signal path during receive mode, this scheme minimizes additive noise.

In Tuning mode, the MCU forward-biases both PIN diodes (D1 and D2). Hence, D1 conducts, and forms a low impedance connection between the phase comparator and the coil. The $\pi$ network acts as a $\lambda/4$ transmission line, so with D2 providing low impedance
to ground, both the coil and phase comparator see a high impedance as they look toward the scanner.

In Receive mode, the MCU reverse-biases D1 and D2. This creates > 30dB of isolation across D1 (into the phase comparator), and enables the passive $\lambda/4\pi$ network to pass the coil’s signal to the scanner.

**Microcontroller**

An Atmel 90S8515, 8-bit microcontroller (MCU) runs the autotuning circuitry. We choose this device for its flexibility and ease of operation, and we use the CodeVision AVR development platform (Bucharest, Romania) to program the MCU in C.

The MCU controls the PLL Synthesizer and an AD—digital-to-analog converter (DAC) via a serial peripheral interface. The DAC provides the DC reverse-bias which sets the coil’s varactor-diode capacitance (and hence, its center frequency).

**Device Operation**

The MCU acts as a simple state machine. At power-up it initializes the DAC and PLL Synthesizer via serial peripheral interface, and enables the current feedback op-amp. By pressing a button, the user changes the device into ‘tuning’ mode, and it sweeps the DAC to sweep the reverse-bias/capacitance of the varactor-diode. The MCU’s on-board analog comparator trips when the phase-comparator outputs 0V (with respect to MCU ground), corresponding to purely real coil impedance at the PLL Synthesizer frequency. This triggers change of state to ‘receiving’ mode, and we power-down the MCU to prevent spurious behavior from gradient switching interference.

**Experimental Procedure**

![Figure 1: Block Diagram of Autotuning Circuitry (in all its fine glory).](image)
Figure 2: PLL Synthesizer Block Diagram. The MCU sets the PLL to generate a signal which requires filtering (4-pole Butterworth) before it dictates the minicircuits VCO to oscillate at the Larmor frequency. The current feedback op-amp (CFB) buffers this signal and drives the coil. The MCU sets the CFB to high-Z during Receive Mode to eliminate interference.

Figure 3: Phase Comparator Circuit Diagram. $C_{ref}$ and the coil share current from the PLL Synthesizer. The ultrafast comparators eliminate amplitude differences between the voltages across $C_{ref}$ and the coil, so the multiplier has a DC term proportional to $\cos(\phi_C - \phi_{coil})$, where $\phi$ is phase of each voltage waveform. $R_{lp}$ and $C_{lp}$ lowpass filter the multiplier output before sending it to the MCU. Note that the resistors ($R = 1.5k\Omega$) on the comparator inputs prevent offset due to input bias currents.
Figure 4: Tune/Receive Switch Circuit Diagram. The MCU sets PIN diodes D1 and D2 to be low-impedance in Tune mode, and high impedance in Receive mode. \( L_\pi, C_{\pi 1} \text{ and } C_{\pi 2} \) form a \( \lambda/4 \) “\( \pi \)” network, mimicking a quarter wavelength of transmission line. When D2 conducts DC current, it provides a near short-circuit on one end of this \( \lambda/4 \). Hence, the coil and phase comparator see a high impedance on the opposite side of the \( \pi \) network. Chokes and DC blocking capacitors isolate the control circuitry from the signal path.